Remarks/Arguments

Rejection of Claims 1-13 under 35 U.S.C. 112

Claims 1-13 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. According to present specification, the purpose of the DRAM cell in Figs 2(A) and 2(B) is to be the charging capacitor for charging and providing the pumping voltage VPP on word line (Please refer to lines 10-18, page 4). Therefore, the DRAM cell should not incorporate with any of word line and bit line inside. Besides, the Fig. 2(B) is amended to show the waveform of clock signal now. Withdrawal of this rejection is respectfully requested.

Rejection of Claims 1-13 under 35 U.S.C. 103(a)

According to paragraphs 5-6 of the Office Action, Claims 1-13 are rejected under 35 U.S.C. 103(a) as being anticipated by Tsukude (US Patent No. 6,205,067). Applicant respectfully submits that such rejection is improper for the following reasons:

Tsukude disclosed the memory blocks MB comprising a plurality of memory cells. Memory cell MC includes a memory capacitor MQ for "storing information", and an access transistor MT formed of an n channel MOS transistor which is turned on in response to a signal potential on a corresponding word line to "connect memory capacitor MQ to a corresponding bit line" (see col. 2, lines 7-13). Nevertheless, the DRAM cell in present application is used to be a charging capacitor for charging and providing the pumping voltage VPP(see page 4, lines 9-18), and then the VPP is provided on word line. The feature that DRAM cell is used as charging capacitor is

claimed in claims 1 and 9.

Secondly, Tsukude disclosed the control clock generator 6 for generating the signal BIAC. The signal BIAC is used to control the address control circuit (see co. 7, lines 54-66). But, the clock signal provided from driving circuit in present invention is used to drive the memory capacitor (see page 4, lines 13-15, 24-26) as claimed in claims 6 and 9.

Finally, Tsukude disclosed the switching circuit 34, including inverter, PMOS transistor 34c and NMOS transistor 34b, for providing the third clock signal Vcp to drive the plate line of capacitor MQ of the memory cell. The purpose of switching circuit disclosed by Tsukude, is to choose one of the Vcpa and the Vcpb voltage to output according to the clock signal BIAC (see col. 17, lines 14-31). Nevertheless, in the embodiments of present invention, the driving circuit would generate the output signals based on the received input signals such as θ_1, β and γ (see page 4, lines 9-27). The purpose of driving circuit is claimed in claims 6 and 9, so difference between present invention and Tsukude is obvious.

For the reasons above, Applicant respectfully requests the withdrawal of ALL the rejections based on Tsukude, either with or without in view of further citation(s).

Conclusion

Having thus overcome the rejections made in this Office Action, withdrawal of the rejections and expedited passage of the application to issue is requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Amendments to the Drawings:

The attached sheets of drawings include changes to FIG. 1, FIG. 2(A) and FIG. 2(B). The sheets, which include FIG. 1, FIG. 2(A) and FIG. 2(B), replace the original sheets including FIG. 1, FIG. 2(A) and FIG. 2(B).

Attachment: Replacement Sheets